EXHIBIT 31

IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS

VLSI TECHNOLOGY LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No. 1:19-cv-00977-ADA

DECLARATION OF DR. ALYSSA B. APSEL
IN SUPPORT OF INTEL CORPORATION'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

I. INTRODUCTION AND QUALIFICATIONS

1. I have been retained by counsel for Intel as an expert consultant in this litigation. In this declaration, I provide my opinions in response to Plaintiff VLSI Technology LLC's Opening Claim Construction Brief regarding the proper construction of the disputed claim terms of the '485 patent.

2. I previously provided a Declaration in Support of Intel's Opening Claim Construction Brief ("Opening Declaration"), in which I described my qualifications, provided an overview of the technology and the '485 patent, and provided my opinions regarding how the disputed terms should be construed. I incorporate my Opening Declaration by reference here.

3. In preparing this Declaration, I have considered VLSI's Opening Claim Construction Brief and the Declaration of Professor Thomas Conte, in addition to the materials I listed in my Opening Declaration.

II. '485 PATENT

A. Disputed Term: "a capacitance structure" (claims 1, 12, 17)

4. As I discussed in my Opening Declaration, at the time of the '485 patent's filing and continuing through today, the term "capacitance structure" would not connote a definite structure to a person of skill in the art.

5. I understand that VLSI has asserted that the term "capacitance structure" refers to a "well-known class of physical structures" that includes "capacitors, transistors connected in a manner to have capacitance, and dummy cells having capacitance." I disagree that the term refers to a "well-known class of physical structures." I am not aware of any treatises, publications, or other references that define "capacitance structure" in terms of those structures. Instead, as I stated in my Opening Declaration, virtually every integrated circuit component has some amount of capacitance, so VLSI's construction would render the term "capacitance" meaningless.

6. I understand that VLSI also has asserted that Intel's proposed construction would render the express reference to "dummy cells" in claims 1 and 12 superfluous. A person of ordinary skill in the art would understand that the express recitation of "dummy cells" in claims 1 and 12 results in those claims having a narrower scope that they would have if they merely recited a "capacitance structure." Specifically, the references to a "plurality of dummy cells" in claims 1 and 12 confirm that the capacitance structure ***must include*** a plurality of dummy cells, rather than covering a broader set of equivalent structures. Claims 3 and 19 both further specify the number of dummy cells coupled to the dummy line. Claim 3 requires that a "plurality" of dummy cells are coupled to the dummy line, and claim 19 requires that one dummy cell is not coupled to the dummy line. *Id.* at 8:1-4, 10:21-28. I understand that these claims are, therefore, narrower in scope than claims 1 and 17, respectively, because they require that the capacitance structure have a specific configuration.

7. I understand that VLSI also asserts that the claims, the specification, and the prosecution history of the '485 patent repeatedly describe how the capacitance structure interacts with the other physical structures in the claimed memory circuit. The claims contain multiple means-plus-function limitations describing circuit elements that couple different circuit components. *Id.* at 10:6-17 (discussing the "coupling" and "decoupling" means). The fact that various circuit components are coupled to other components, does not describe the structure of the circuit components themselves. Accordingly, a person of ordinary skill would understand the fact that the capacitance structure is "coupl[ed]" to the second power supply line or to "transistors" does not to provide any information about the structure of the capacitance structure itself.

B. Disputed Term: "precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells" (claim 17)

8. As I discussed in my Opening Declaration, Intel identifies the corresponding structure as:

> (1) voltage source V_{REF} and transistor 36, coupled in series to provide a reference voltage to one or more dummy cells through conductor 37, as shown in Figure 2, and equivalents thereof; or alternatively (2) voltage source V_{REF} and transistor 90, coupled in series to provide a reference voltage to one or more dummy cells through conductor 71, as shown in Figure 3, and equivalents thereof.

9. Each component identified by Intel is necessary to perform the claimed precharging function.

10. I understand that VLSI asserts that voltage source V_{REF} and the transistor are not necessary to perform the precharging function. VLSI Br. 13. I disagree. As I explained in my Opening Declaration, the specification clearly links each of the components identified by Intel to the function of precharging, and each component is necessary for precharging.

11. The claimed precharging function requires setting the voltage of the capacitance structure to a particular level, which requires the voltage reference source to act as a power supply to charge the capacitance structure. *Id.* at 4:7-14 ("The conductor 37 is coupled to receive a reference voltage labeled 'V_{REF}' via an N-channel transistor 36."); *id.* at 4:28-33. Moreover, if the transistor were not present, the conductor would always be connected to the voltage reference source, which would fix the voltage of the dummy cells and conductor at the reference voltage. In that case, if the line of memory cells being written to were coupled to the conductor, no charge sharing would occur. Instead, any charge would travel from the reference voltage source though the conductor to the memory cells being written to.

C. Disputed Term: "first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" / "second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" (claim 17)

1. VLSI's proposed "switching circuit"

12. As I discussed in my Opening Declaration, the specification does not disclose the structure for a "switching circuit" that performs the claimed function. I understand that VLSI has pointed to the language in the specification at 6:47-59 stating that:

> A switching circuit that has transistors that, when the second line of memory cells is selected for writing, couple the first power supply terminal to the first power supply line, decouple the first power terminal from the second line of memory cells, and couple the second power supply line to the first capacitance structure.

See also, id. at Abstract. This language merely paraphrases the language of claim 17 and does not disclose the structural features of such a circuit. *Id.* at Abstract, 6:47-59 (cited in VLSI Br. 15-16).

2. Intel's proposed "first coupling means"

13. As I discussed in my Opening Declaration, Intel identifies the corresponding structure as:

> (1) transistor 52 and clamping circuit 46, configured to couple power supply voltage V_{DD} and conductor 35, as shown in Figure 2 (if the second line of memory cells is SRAM column 15), and equivalents thereof; or alternatively (2) transistor 96 and a clamping circuit, configured to couple power supply voltage V_{DD} and conductor 67, as shown in Figure 3 (if the second line of memory cells is SRAM row 68), and equivalents thereof

14. Each component identified by Intel is necessary to perform the claimed precharging function.

15. I understand that VLSI asserts that the structure identified by Intel does not perform the claimed function because the transistors are decoupled during the write operation. VLSI Br. 17-18. VLSI's argument confuses which column of cells is being written to when. As the '485 patent explains, transistors 52 and 96 decouple the power supply from their respective lines of memory cells ***only*** when their lines of memory cells are being written to. '485 patent at 4:33-44, 6:16-27, 4:52-53. When their lines of memory cells are not being written to, the transistors ***couple*** the power supply terminal to the line of memory cells. In claim 17, the "first coupling means" couples a line of cells that is not being written to the power supply terminal. This is exactly the function performed by the structure identified by Intel.

16. I understand that VLSI further asserts that the clamping circuit does not perform the coupling function and instead "function[s] to limit the voltage drop" on the power supply line. VLSI Br. 18. However, the clamping circuit is able to limit the voltage drop on the power supply line because it couples the power supply terminal to the power supply line. If the clamping circuit were not coupled between the power supply terminal and the power supply line, it would not be able to limit the voltage drop. Thus, the fact that the clamping circuit is able to perform the clamping function actually supports Intel's argument that the clamping circuit performs the claimed coupling function.

Date: November 18, 2019

Alyssa B. Apsel, Ph.D.